Recent progress in SiC single crystal wafer technology

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ABSTRACT
This paper reviews recent developments in silicon carbide (SiC) single crystal wafer technology. The developments include the attainment of wafer diameters up to 100 mm and micropipes with densities less than 1 cm\(^{-2}\) on 4H-SiC wafers with a diameter of 100 mm. Furthermore, high-quality SiC homoepitaxial thin film growth has been achieved, and owing to the availability of large high-quality epitaxial wafers, SiC power devices have begun to show performance levels that largely exceed those produced from Si. In this paper, the problems faced in the development of large high-quality SiC wafers are overviewed in the light of recent achievements.

INTRODUCTION
Global warming and the remarkable rise in oil prices have made the development in energy-saving technologies imperative. In particular, the efficient use of electricity is of paramount importance since it is the most widely used energy source at home and in the industry. In this respect, an improvement in the performance of power semiconductor devices is critical. Today, these devices are used in nearly everything – from home appliances to automobiles, and therefore, it is necessary to enhance their efficiency. For this reason, the limitations of the material properties of present-day Si power devices are currently being debated, and wide band gap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) have attracted considerable attention.

The technological potential of SiC for power device applications stems from its outstanding physical and electronic properties [1]. A large band gap (roughly three times that of Si) enables device operation at an increased temperature (600\(^{\circ}\)C for transistors) and with low leakage currents. SiC can withstand high electric fields before breakdown, ten times greater than what Si can endure, and also high current densities. The high electron saturation velocity enables SiC to generate high power at high frequencies. SiC has excellent thermal conductivity, larger than that of copper at room temperature, which makes it suitable for high power operation.

In the last decade, SiC crystal growth technology has achieved significant progress and enabled the growth of high-quality, large-diameter SiC crystals. The availability of large-diameter SiC single crystals has resulted in the rapid progress in SiC thin film epitaxy and device fabrication. Several device prototypes have already been demonstrated, which include PiN rectifiers with a blocking voltage of 19 kV [2], Schottky barrier diodes (SBDs) with an extremely low recovery current [3], MOSFETs with a blocking voltage of 700 V at a specific on-resistance of 1.8 m\(\Omega\)cm\(^2\) [4], and SiC commutated gate turn-off thyristors that operate at a current rating of 150 A, with which 180 kVA inverter has been successfully operated [5]. Since 2001, SiC SBDs have been commercially available and applied to several power electronic systems such as switched-mode power supplies and industrial frequency inverters.

In this paper, I will overview the recent developments in SiC single crystal wafer technology. In particular, I will describe the issues pertaining to the enlargement of the active area of SiC devices to allow high-current operation. The technology has shown rapid progress, and further developments are expected in high efficiency SiC power devices and systems.

SiC CRYSTAL GROWTH
SiC bulk crystals are almost always produced by a physical vapor transport (PVT) growth process; in this process SiC source powder sublimes and is recrystallized on a slightly cooled seed crystal at uncommonly high temperatures (> 2400\(^{\circ}\)C). The growth is generally conducted on a SiC \{0001\} platelet or wafer, resulting in a crystal growth direction being parallel to the \(<0001>\ c\)-axis. The extremely high process temperature for SiC bulk crystal growth gives rise to increased difficulty in growing high-quality crystals as the crystal diameter increases, and the successful development of the diameter-enlargement process has been a key issue for the SiC bulk crystal growth technology.

The growth of high-purity SiC homoepitaxial thin films on SiC single crystal wafers is required to obtain \(n/n^+\) wafer structures for power device applications. For the epitaxial growth of SiC, chemical vapor deposition (CVD) is advantageous in that the epitaxial layer thickness and impurity doping can be precisely controlled and made uniform. Several trials of SiC CVD were performed in early days, but a serious problem of 3C inclusions hindered the successful deposition of high-quality SiC thin films. In the late 1980s, a group at Kyoto University developed a new technique called “step-controlled epitaxy” [6], in which surface steps introduced by vicinal \{0001\} substrates allowed the deposited thin films to succeed the stacking sequence (polytype) of the underlying
WAFER FABRICATION
Wafer fabrication is a process that is employed for manufacturing SiC wafers with a desired crystal surface orientation and is indispensable for the practical application of SiC crystals to power semiconductor devices. From the viewpoint of the application to power semiconductor devices, the wafer fabrication process is evaluated according to the following two criteria: (1) shape and thickness variation of the wafer, and (2) crystallographic integrity of the wafer surface. In particular, to obtain SiC devices with a high current rating, the wafer geometry (wafer flatness) is extremely important since advanced power semiconductor devices require fine device patterning over a large device area.

Highly flat SiC single crystal wafers have recently been fabricated by employing a double-side lapping technique [7]; in this technique, a four-step lapping process consisting of four stages of double-side lapping with different grit-size abrasives is employed, and the process enables an excellent flatness with a total thickness variation (TTV) of less than 3 μm and local thickness variation (LTV) of less than 1 μm over the entire surface area of three-inch 4H-SiC wafers to be obtained.

For the surface quality improvement, several methods such as mechano-chemical polishing (MCP) with colloidal silica (CS)-based slurry [7,8] and a catalyst referred etching (CARE) method [9] have been carried out. The CARE method is a planarization etching process that uses a reference plane fabricated from a catalyst such as Pt and Mo, which generates reactive species, while the MCP method employs a combination of conventional CS slurry and adequate oxidizers. Both the methods allow us to obtain an excellent surface smoothness, i.e., as low as Ra ~ 0.1 nm. Figure 1 shows two- and three-inch 4H-SiC wafers fabricated by an MCP process (courtesy of Nippon Steel Corporation).

CRYSTAL DEFECT REDUCTION
(A) MICROPPIPES
One of the major problems with SiC wafers pertains to the so-called “micropipes,” which are large Burgers vector screw dislocations with a small pinhole. They penetrate the entire crystal along the c-axis and cause critical flaws in SiC devices. Micropipes are interpreted in the framework of Frank’s model of hollow core dislocations [10]. Figure 2 shows an atomic force microscope (AFM) image of the (0001)Si surface of 6H-SiC, where a spiral step ending at a micropipe is visible. The almost archimedean circular spiral step is characterized by a large step height (13.5 nm corresponding to nine times the unit c lattice parameter of 6H-SiC) because of the large Burgers vector of the micropipe.

Several possible causes exist for the formation of micropipes, and they are categorized into three groups: (1) thermodynamic, (2) kinetic, and (3) technological causes. For example, the thermodynamic causes include thermoelastic stress due to non-uniform heating, while the kinetic causes are related to the nucleation process and growth surface morphology. In all these cases, one must also consider the technological aspects, such as the seed surface preparation and contamination of the growth system.

Recent advances in the PVT growth technique have made possible a highly-controlled growth process for SiC bulk crystals and enabled us to achieve reproducible crystal growth under optimized growth conditions, which has led to a continuous reduction in the micropipe density over the past several years. Recent demonstration of extremely low micropipe densities (less than 1 cm⁻² or even zero) over 100 mm diameter SiC wafers [11,12] is expected to lead to the enhancement in the yield and productivity of SiC power devices, and thus reducing their costs.
(B) EPITAXIAL DEFECTS

As mentioned above, a successful reduction in the micropipe density has been achieved, and the fabrication of large active area SiC devices is being intensively pursued. However, the yield of large active area devices appears still limited for devices larger than several millimeters square. On the basis of this device size dependence, the density of killer defects in SiC wafers is estimated to be around few per square centimeter. The most plausible candidate for the defects is epitaxial defects that are process-induced defects occurring during the epitaxial thin film growth of SiC.

In most cases, the epitaxial defects are generated at the epitaxial film/wafer interface. They extend along the step flow direction during the epitaxial growth (parallel to the off direction of wafers) and are categorized by their surface morphological features emerging on the as-grown epitaxial film surface and referred to, e.g., as carrots and comet tails. Figure 3 shows an optical micrograph image of a carrot defect observed on the epitaxial film surface grown on a 4H-SiC wafer 8° off-oriented toward [1120]. Through synchrotron x-ray topography and TEM studies, it is confirmed that the carrot defects have a Frank-type stacking fault on the basal plane connected to a prismatic fault [13]. Their formation is assumed to be closely related to threading screw dislocations (TSDs) in the underlying SiC wafers. One important aspect here is that the typical density of TSDs (few thousand per square centimeter) largely differs from that of carrot defects, which is usually in the range of few per square centimeter. This implies that other factors rather than the existence of TSDs largely affect the occurrence of carrot defects. Although it is yet to be confirmed, it is suggested that basal plane dislocations (BPDs) existing in the close vicinity of TSDs contribute to the formation of carrot defects [14,15].

Epitaxial defects have a negative impact on the SiC power devices, and thus, their reduction has been a major issue in the study of SiC epitaxial growth. The mechanism through which these defects adversely affect the performance of SiC devices is yet to be clarified. A possible explanation for the degradation of devices is that the defects contain extended stacking faults on the (0001) basal plane. The stacking faults in hexagonal SiC generally give rise to a local cubic (3C) stacking sequence along the c-direction, and this 3C inclusion brings about spatial inhomogeneity in the electrical conductivity of the material. The strong electrical anisotropy owing to basal plane stacking faults in SiC crystals was first reported by Takahashi et al. [16]. They examined 6H- and 4H-SiC crystals grown in the [1100] direction, which exhibited stacking fault densities between $10^2$ and $10^4$ cm$^{-1}$. It was found that SiC crystals with such a high stacking fault density showed a very weak temperature dependence of the resistivity parallel to the stacking faults at low temperatures, indicating the existence of two-dimensional electron gas (2DEG) at the stacking faults. Later Iwata et al. [17] lent support to this conclusion; using first-principles theoretical calculations, they revealed a quantum-well-like feature of 3C inclusions in hexagonal SiC crystals with a relatively large conduction band offset between the cubic and the hexagonal polytypes, which gives rise to 2DEG at the stacking faults.

Fig. 3. Optical micrograph of a carrot defect observed on the epitaxial film surface grown on a 4H-SiC wafer 8° off-oriented toward [1120].

(C) DISLOCATIONS

Another important issue relating to the SiC single crystal wafers is the dislocations that are present in currently commercially available SiC wafers; the densities of the dislocations are on the order of thousands per square centimetre, which are nearly 10000 times the micropipe densities. The dislocations in the SiC crystals are
classified into two groups depending on their propagation direction. One group comprises threading dislocations propagating approximately along the crystal c-axis, while the other consists of the BPDs lying in the (0001) basal plane. Most of the threading dislocations in PVT-grown SiC crystals are grown-in type dislocations and are introduced by the growth process. They are often introduced in the initial nucleation stage of the crystal growth and may also be caused by secondary phase and/or foreign polytype inclusions. On the other hand, the BPDs are believed to be caused by thermoelastic stresses exerted on the crystal during the growth and/or post-growth cooling, since for hexagonal SiC crystals, the basal plane (0001)<1120> glide system is easily activated at high temperatures.

While not nearly as detrimental to SiC devices as micropipes, it has recently been demonstrated that dislocations in SiC crystals degrade several characteristics of SiC devices, e.g., the blocking capabilities of SiC SBDs and the forward bias characteristics of SiC PiN diodes. In addition, dislocations also influence the device performance through the formation of epitaxial defects. In particular, TSDs are of most serious concern since they often trigger carrot defect formation. Generally, the epitaxial growth process proceeds by the step flow mechanism on the off-oriented (0001) surface. TSDs are likely to interfere with this step flow mechanism. During epitaxial growth, steps propagating in the off-direction interact with spiral steps originating from TSDs on the growing wafer surface. This step interaction can cause the stacking disorder at the growth front and result in epitaxial defects (e.g., carrots) during the epitaxial process.

As mentioned above, most TSDs arise due to growth instabilities during the PVT growth process, especially in the initial stage of the growth process. The typical density of the TSDs is around few thousand per square centimeter. It has been reported that the density and distribution of the TSDs significantly change during the bulk crystal growth of SiC. There is a 30–70% decrease in the TSD density along the length of the crystal [18,19]; this observation is often accompanied by a significant redistribution of TSDs over the grown crystal surface [19]. Recently, the PVT growth process of SiC has shown considerable progress, and under optimized growth conditions, the TSDs with densities of less than 200 cm$^{-2}$ have been successfully obtained for three-inch diameter 4H-SiC wafers [12].

BPDs have also drawn increased attention ever since it was revealed that they degrade not only the forward bias characteristics of SiC PiN diodes but also the gate oxide reliability of SiC MOSFETs. BPDs are, in general, introduced by thermoelastic stresses during the crystal growth and/or post-growth cooling process. The density of BPDs is increased via multiplication processes that are activated at high temperatures, where the interaction between BPDs and threading dislocations plays a vital role [20,21]. Another important aspect of BPDs is the occurrence of a dislocation conversion process during the SiC epitaxial growth, which has been first reported by Ha et al. [22] and has been intensively investigated over the last several years. During the epitaxial growth of SiC using CVD, BPDs in the wafers are converted into threading edge dislocations (TEDs) in the epilayers. This conversion was considered to be a result of the image force effect in the epilayer between the flowing growth steps and the BPDs. A majority of the BPDs in the wafers are converted into TEDs in the subsequently grown epilayers.

The dislocation conversion process has a technological advantage: it reduces the BPD density in the SiC wafers. Deliberate surface preparation significantly enhances the probability of the BPD to TED conversion, and pre-growth surface etching by molten KOH reduces or even fully eliminates BPDs from the epitaxial layers [23]. In recent years, other types of defect conversion processes occurring during the SiC crystal growth process have also been reported, which include TED to BPD [24] and TSD to Frank type stacking fault conversions [25]. Figure 4 schematically shows some of the dislocation-related processes occurring during the SiC epitaxial growth. Although most of the conversion processes have been reported for epitaxial thin film growth, they can also be operative during the PVT growth of the SiC bulk crystals.

**SUMMARY**

This paper reviewed the current status of SiC single crystal wafer technology and some remarkable developments in the technology. In this study, I overviewed important technological advances in the SiC wafer technology and discussed problems that are yet to be addressed. For the implementation of advanced SiC power devices, it is important to further improve the SiC single crystal wafer technology, leading to the development of SiC wafers with large diameters and better crystalline quality at reasonable costs.

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**REFERENCES**


