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Comprehensive Upstream Silicon Processing for Semiconductor and Solar Applications

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Abstract

A majority of modern microelectronic devices and solar cells are built on silicon substrates or substrates derived from silicon. Upstream silicon processing involves the manufacture of silicon substrates for semiconductor and solar applications. The production of semiconductor wafers and the production of solar wafers share a few common unit operations and physical phenomena at different scales. Hence, the solar wafer manufacturing is discussed as a subset of the semiconductor wafer manufacturing. This paper addresses key unit operations and physical phenomena relevant for the manufacture of silicon wafers, from polysilicon production to final polishing, followed by wafer defect engineering. The present condition of the silicon processing industry and its evolution in the context of changing market dynamics are discussed in brief. The discussion is broad and panoramic.

Introduction

The electronic revolution marked key technological advancements in the second half of the 20th century. During this period, the world became increasingly dependent on electronic equipment and the information technology. Computers, cellular phones, electronic gadgets and equipment play a critical role in the very functioning of modern society. A majority of electronic equipment are built on silicon based microelectronic devices. Silicon was as important to the semiconductor and electronic revolution as steel was to the industrial revolution.

Perhaps, the 21st century will be defined by the revolution in the energy technology (ET). The alarming environmental effects and limited supply of the fossil fuels are driving our research for alternative energy sources. At present, solar energy harvesting using silicon is becoming increasingly popular. Hence, silicon is expected to play an important role in the energy technology revolution as well.

The semiconductor industry is growing approximately at an annual rate equal to 10%, but the solar silicon sector is exploding at an annual growth rate approximately equal to 40% [1]. Although these growth rates are not sustainable in perpetuity, the innovations in the semiconductor industry and the energy technology are expected to keep the demand for raw silicon at a very high level.

Silicon processing for semiconductor applications and silicon processing for solar applications share many unit operations and fundamental physical phenomena. Polycrystalline silicon, also known as polysilicon, produced by the chemical deposition of silicon from its compounds in either fluidized bed reactors (FBRs) or Siemens reactors, is the starting material for the fabrication of both solar cells and microelectronic devices. Highly pure polysilicon is used to grow silicon single crystals for the production of semiconductor silicon wafers. The production of semiconductor silicon substrates typically involves silicon single crystal growth by the Czochralski (CZ) process, slicing operation that cuts cylindrical crystals into circular wafers, various mechanical wafer shaping processes, chemical etching to remove the mechanical damage near wafer surfaces, and surface polishing (Figure 1a). The production of solar silicon wafers involves the growth of silicon multicrystals by the directional solidification, mechanical slicing of multicrystals to produce rectangular wafers, and chemical etching of wafers (Figure 1b). This paper addresses salient features of both solar and semiconductor silicon processing, by taking a broad view.

Production of Polysilicon

The emerging solar silicon industry has significantly increased the demand for polysilicon. The demand for polysilicon is expected to exceed its supply during the next few years and grow in foreseeable future [1]. Hence, an effective and rapid production of polysilicon has become the most important technical and business goal for a

majority of silicon producers. Polysilicon is traditionally produced by the Siemens process by the deposition of silicon from trichlorosilane (TCS) on silicon rods [2]:

$$SiHCl_3 + H_2 \rightarrow Si + 3HCl \qquad (1)$$

The advantage of the Siemens process is its simplicity. TCS is passed over silicon rods at high temperatures (around 1100 ^{0}C to 1200^{0}C) to trigger the chemical deposition of silicon. The deposition process itself is quite complex and involves many elementary reactions. The productivity of silicon, however, is relatively low, as the kinetics of the deposition is slow at lower temperatures and the deposition is strongly influenced by the reagent mass-transport effects. Moreover, the surface area available for the deposition per unit volume of the reactor is very low. Hence, there are incentives to explore alternative processes that can more effectively satisfy increasing demand for polysilicon.

Fluidized bed reactors (FBRs) provide an excellent platform for an effective production of polysilicon [3-7]. A fluidized bed reactor is a vertical cylindrical reactor, in which solid particles are in continuous fluid-like motion, induced by the friction between particles and gases that pass through the reactor [8]. Gases are introduced from the bottom of the reactor. Although it is not necessary, it is convenient to understand the dynamics of FBRs under isothermal conditions, assuming constant gas properties. As the inlet gas velocity increases, the friction between gases and particles increases. When the bed weight (solids or particles) is balanced by the frictional drag, the bed is suspended or *fluidized*. At the onset of fluidization, solid particles are *lifted* by the gas-solid friction. Gases move in the interstitial region between solid particles. The fraction of the reactor volume occupied by gases at the onset of fluidization is termed *the minimum fluidization bed voidage* or E_{mf}. The gas velocity at the minimum fluidization or the onset of fluidization is called the *minimum fluidization velocity* or U_{mf}. A fluidized bed reactor provides excellent gas-solid contact, very high gas-solid heat and mass-transfer rates, and high particle surface area per unit volume of the reactor. Thus, the productivity of multiphase systems involving gas-solid reactions is very high in fluidized bed reactors.

Typically, silicon from silane is deposited on silicon particles in fluidized bed reactors at around 650 ^{0}C [3]:

$$SiH_4 \rightarrow Si + 2H_2 \qquad (2)$$

The rate of deposition of silicon from silane on silicon particles is higher than the rate of deposition of silicon from TCS. Thus, chemical vapor deposition (CVD) at lower temperatures is possible with silane. In the fluidized bed reactors (FBRs) producing silicon from silane, the incoming gases are silane and hydrogen. Hydrogen is used to control the silane concentration and maintain the fluidization of silicon particles. At the minimum fluidization, however, the gas flow rates are not as high as desired. Moreover, it is difficult to operate an FBR at the minimum fluidization condition, without settling the particles. Hence, higher gas flow rates are desired to achieve higher productivities and for safer operation. As the gas flow rate increases beyond U_{mf}, however, the excess gas contributes to the formation of gaseous bubbles, increasing the *bed voidage*. From a phenomenological point of view, an FBR can be assumed to consist of bubbles and an *emulsion* containing gases in contact with solid particles. The quality of the emulsion is quite similar to the quality of the reactor bed at the minimum fluidization condition. The local voidage in the emulsion is close to the minimum fluidization bed voidage; bubbles can be assumed to be generated by the gas introduced in excess of what is required to achieve the minimum fluidization. As the ratio of the actual gas velocity (U) to the minimum fluidization velocity (U_{mf}) increases, the bubble formation intensifies. At a very high U/U_{mf}, large slugs of gas are formed in the reactor. It is noted that FBRs operate under chaotic conditions. Hence, only a time-averaged steady state for an FBR can be defined.

To understand the dynamics of FBRs, it is necessary to study different reactions in the silane-silicon system. Figure 2a shows the reactions of interest in the silane-silicon system. Reaction (1) represents the heterogeneous deposition of silicon from silane on silicon particles, which is the primary reaction of interest. Silane also produces silicon vapor (Reaction 3), which homogenously nucleates to form silicon fines (Reaction 4). Fines can grow by the diffusion of silicon vapor (Mechanism 5) and by the chemical deposition of silicon from silane (Reaction 2). It must be noted that Reaction (2) is kinetically and mechanistically the same as Reaction (1), which involves the deposition of silicon from silane on silicon particles. Smaller fines can coagulate into larger fines (Reaction 7). Fines can be scavenged by silicon particles (Reaction 8). Particles can grow by the diffusion of silicon vapor (Mechanism 6), in addition to the

chemical deposition of silicon from silane (Reaction 1). The described reactions do not constitute an entire set of elementary reactions taking place in this complex system but represent the system mechanistically.

It is evident that a higher gas (silane + hydrogen) flow rate is desired to achieve a higher silicon productivity; but, as the bed voidage increases with the gas flow rate, the contact between silicon particles (solids) and the gases becomes less effective. For a given volume of the reactor, the surface area of particles in contact with the reacting gases decreases with increasing bed voidage. This, along with the reduced gas residence time, contributes to a reduction in the silane conversion. Since both the dust (fines) formation (and growth) and the particle growth compete for the same source (silane), the local number density of particles strongly influences this competition. Significant fines formation and growth can occur in bubbles or slugs, where silicon particles are absent. Obviously, manipulating the dynamics of an FBR, the gas-solid contact, and operating conditions is critical to maximize the deposition of silicon and minimize the formation of fines. Figure 2b shows the simulated snapshot of a silane mass-fraction field in a typical fluidized bed reactor. The simulation is rigorous, treats all gases as compressible, and accounts for the changes in the molar flow rate of the gaseous mixture caused by the reactions.

Fluidized bed reactors offer an opportunity to meet the demand for polysilicon in future. They are capital intensive but cost effective in the long term. It is noted that the purity of polysilicon required for the production of semiconductor wafers is very high compared to that required for the production of solar wafers. The processes involved in the purification of reactants and products are not discussed in this paper for the sake of brevity.

Crystal Growth

Silicon used in semiconductor processing must be pure, monocrystalline and free of large crystallographic imperfections. The total number of customized quality specifications for semiconductor silicon wafers required by the microelectronic device manufacturers has increased from around 1,200 in 1990 to more than 2,200 in 2008, and is expected to increase further in future [1]. These specifications address materials properties, mechanical properties, and geometric features of the substrate silicon wafers. The intrinsic quality of a wafer is primarily determined by the intrinsic quality of the parent silicon crystal. Hence, crystal growth is among the most important unit operations in silicon processing.

Semiconductor silicon single crystals are popularly produced by the Czochralski (CZ) process. This process allows the continuous growth of a silicon crystal from hot silicon melt placed in a quartz crucible. The Czochralski crystal growth is a complex process involving industrially relevant multiscale and multiphysics phenomena. The dynamics of crystal growth is better understood by both experimental observation and theoretical analysis. The evolution of various microstructures in a crystal, the primary indicators of the crystal quality, is strongly influenced by the crystal temperature field. The crystal temperature field is coupled with the melt flow field, the melt temperature field, and the temperature fields in all parts of the crystal puller. A simultaneous quantification of this three-dimensional complex system is computationally expensive. Although these computations have been accomplished, for the sake of simplicity, reasonable decoupling approaches are often adopted [9-15].

The crystal temperature field, especially in the vicinity of the melt/crystal interface, significantly influences the crystal quality by influencing the evolution of microstructures known as microdefects [16-21]. Hence, the control of the interface shape itself is very critical. In a coupled system like this, it is still possible to develop a modular cause and effect framework for the process development. For example, the melt flow field can be viewed to influence the melt/crystal interface in such a way that the interface shape can be controlled by the manipulation of the melt flow field. The gross characteristics of the melt flow field depend on the operating conditions. The direction of the rotation of the crystal and the crucible containing the melt strongly influence the interface shape. In the co-rotation condition, the crystal and the crucible rotate in the same direction and the crystal typically rotates at a higher rate. Under this condition, the melt flow is characterized by two dominant flow vortices or cells on the meridional plane, as shown in Figures 3. The flow below the crystal is driven by the centrifugal pumping and the flow near the crucible wall is driven by the natural convection. Understanding the driving forces of these flow vortices provides insights into how heat is transported within the melt and how the melt/crystal interface shape can be influenced. The centrifugal pumping results because the magnitude of the radial pressure gradient is lower than the centrifugal force, close to the crystal. This imbalance is caused by the difference between the angular rotation rate of the melt below the crystal and the angular rotation rate of the main body of the melt. Under the counter-rotation condition, the crystal and the

crucible rotate in opposite directions. A typical temperature field and a typical flow field in the melt, developed under the counter rotation condition, are shown in Figures 3c and 3d, respectively. Right below the interface, the flow is driven by the centrifugal pumping, creating a small flow vortex; this vortex is often too small to be detected. The large vortex that occupies the central region of the melt extending all the way to the crucible bottom is also driven by the imbalance between the magnitude of the radial pressure gradient and the centrifugal force; in this case, the magnitude of the radial pressure gradient is greater than the centrifugal force. The vortex driven by the natural convection develops close to the lateral wall of the crucible. Hence, it is possible to manipulate the crystal and the crucible rotation to control the flow field in the melt and influence the shape of the interface. The melt flow can also be influenced by the magnetic field. Silicon melt is a moving conductor. Hence, it can generate a body force, known as the Lorentz force, in the presence a magnetic field. Magnetic fields are popularly applied in Czochralski crystal growth.

The quality of a crystal is also influenced by the distribution of dopants and impurities such as oxygen. A few dopants are intentionally added to alter the electrical properties of the crystal; oxygen is incorporated from the quartz crucible by its transport through the melt. Oxygen provides mechanical strength and primarily interacts with the intrinsic point defects of silicon to influence the evolution of microdefects in silicon. Control of the melt temperature field and the flow field by the manipulation of the crystal rotation, crucible rotation, and magnetic field is critical in controlling the impurity distributions both in the melt and the crystal.

Sophisticated silicon single crystal growth is not necessary for the production of solar multicrystals. Solar multicrystals are produced by the directional solidification of silicon melt (Figure 4). It is necessary to have large grains in multicrystals to produce efficient solar cells. Hence, impurity control in silicon melt to reduce the number of heterogeneous nucleation sites and the temperature field control are necessary. The benefits of increasing the solidification rate and the costs of decreasing the grain size with increasing temperature gradients near the interface must be assessed together.

Czochralski Defect Dynamics

A silicon crystal grown by the Czochralski (CZ) process contains various crystallographic imperfections termed microdefects. Most common microdefects in CZ silicon are the aggregates of self-interstitials known as *A* and *B* defects, the aggregates of vacancies known as *D* defects, and the aggregates of oxygen, primarily silicon dioxide, termed oxygen clusters. These microdefects vary in size from a few nanometers to hundreds of nanometers and can affect the yield of microelectronic devices. Hence, modern device makers require silicon substrates free of large microdefects. Engineering the growth of large-microdefect-free crystals is the most critical part of meeting the challenges posed by the shrinking feature size of microelectronic devices.

The formation of microdefects is influenced by a complex interplay between the transport of the intrinsic point defects of silicon (vacancies and self-interstitials) and impurities such as oxygen, and various reactions involving the intrinsic point defects and oxygen [20-21]. The key reactions dictating the CZ defect dynamics are

$$i + v \rightleftarrows \mathrm{S}i \qquad (3)$$

$$v + O \rightleftarrows vO \qquad (4)$$

$$vO + O \rightleftarrows vO_2 \qquad (5)$$

$$P_{m_x} + x \rightleftarrows P_{(m+1)_x} \qquad \{x = i, v\} \qquad (6)$$

$$O + P_{m_O} + \gamma v + \frac{1}{2} Si \rightleftarrows P_{(m+1)_O} \qquad (7)$$

where *i* denotes self-interstitials and *v* vacancies. A cluster containing *m* units of any species or monomer *x* is denoted by P_{m_x}. The formation of *D* defects (*v*-clusters) in a crystal requires the supersaturation of the crystal with vacancies and the formation of *A* and *B* defects (*i*-clusters) requires the supersaturation of the crystal with self-interstitials. Oxygen clusters (*O*-clusters) are primarily formed under the vacancy supersaturation. This is because the formation of *O*-clusters generates compressive stress that is relieved by the consumption of vacancies by *O*-clusters. The microdefect distribution in a crystal is significantly influenced by its temperature field and pull-rate. Hence, the

microdefect distribution in a crystal can be controlled, by manipulating its temperature field and pull-rate Figure 5 shows the size distribution of various microdefects in a crystal pulled by a varying rate.

Various impurities can be added to a crystal to influence the distribution of microdefects. Nitrogen is a popular impurity used to reduce the size of *D* defects. Nitrogen influences the microdefect distribution by primarily interacting with vacancies [22-23]. A thorough understanding of the Czochralski defect dynamics and the transport phenomena in silicon melt is necessary to develop a crystal growth process capable of producing silicon crystals free of large microdefects.

Silicon Wafering Processes

A series of mechanical and chemical processes are required to produce semiconductor silicon substrates from a crystal, for microelectronic device fabrication. A silicon crystal is first sliced into circular wafers. These wafers are then sequentially treated by various other mechanical shaping operations, chemical etching, polishing, and cleaning processes before they are supplied for device fabrication or wafer defect engineering, described in the next section (Figure 1). The essential quality indicator of all wafering processes is the surface topography quantified at different wavelengths. The most popular topography measures are the roughness, the nanotopography, and the flatness. The amplitude of the roughness is typically measured over a wavelength of less than 100 micrometers, the amplitude of the nanotopography is typically measured over a length of a few millimeters (0.5 mm to 10 mm), and the amplitude of the flatness is typically measured over a length of many millimeters to wafer diameter (15 mm to 300 mm).

After its Czochralski growth, a silicon crystal is sliced simultaneously into many wafers by the mechanical abrasion caused by a moving parallel assembly of wires lubricated by an abrasive slurry. This process does not allow an accurate control of the topography of sliced wafers, at a fine scale. Gross characteristics of the wafer shape such as the warp of a wafer, defined as the difference between the maximum distance between the median surface of the wafer and a reference plane and the minimum distance between the median surface and the reference plane, can be strongly influenced by the slicing process. The warp of a sliced wafer can be approximately quantified by quantifying the local deviations of the parent silicon crystal at the cutting locations, during slicing. This requires the quantification of the temperature field in the crystal along with the induced stress and strain fields [24]. Understanding the sources of warp can help improve the slicing process. Figure 6 shows the observed warp and the predicted warp of a sliced wafer.

A decade ago, a majority of sliced wafers were lapped by abrasive slurries, etched, and polished only on the so-called front side; the back surface of wafers remained etched. This process flow does not yield the excellent topography required for the fabrication of modern microelectronic devices. Etching of silicon wafers by the popular acidic etching solution, a mixture of hydrofluoric acid, nitric acid and a few diluents, is strongly influenced by the reagent mass-transport effects [25-27]. Since perfectly uniform mixing conditions cannot be created in an etching chamber, acid-based etching degrades the wafer flatness. In addition, etching produces gaseous products that mask the wafer surface over a finite timescale, inducing additional degradation of the wafer topography (Figures 7a and 7b). The extrinsic bubbles used to improve mixing uniformity in an etching bath also induce the degradation of the wafer topography (Figures 7a and 7c). Moreover, old front side polishing processes that followed an acid etching process transferred backside disturbances of a wafer to its front side, degrading its front side topography.

To meet the requirements of the modern microelectronic industry, nowadays, silicon wafers are treated by a different set of processes. After slicing, wafers are ground on both surfaces, etched in a solution of potassium hydroxide, a process not significantly influenced by the transport effects, and polished simultaneously on both sides. Several wafers are polished simultaneously in a polisher. Polishing takes place by both mechanical and chemical effects. Wafers rotate about three different axes during polishing to allow for uniform mechanical and chemical removal (Figure 8a and 8b). The wafering processes continue to push the operational limits to meet new quality requirements.

Wafering of a solar multicrystal is relatively simple compared to that of a semiconductor crystal. Solar multicrystals are typically rectangular blocks. These blocks are cut into smaller blocks and then sliced into rectangular wafers by wiresaw as described in this section. These wafers are then etched before the fabrication of solar cells. The challenge in solar wafering is not in meeting the quality specifications but in developing cost-effective processes.

Post-Wafering Defect Engineering and New Materials

Engineering the production of silicon crystals free of large microdefects to meet the needs of the modern microelectronic industry was discussed in the fourth section of this paper. Often, growing such crystals is difficult and expensive. It is easier to grow crystals containing *D*-defects at a higher rate. Since only a narrow region near the front surface of a silicon wafer must be large-microdefect-free, it is possible to reduce the size of *D*-defects in a silicon wafer by annealing it at high temperatures. The high temperature annealing of a wafer provides the necessary driving force for the dissolution of *D*-defects near the wafer surface and creates a large-microdefect-free zone [28]. *D*-defects formed in a crystal grown at a high rate are very large, however, and require a long annealing time, rendering the annealing process economically unattractive. This problem can be addressed by doping silicon melt with nitrogen during crystal growth, which reduces the size of *D*-defects in the grown crystal. Nitrogen strongly binds with vacancies in the crystal to reduce the size of *D*-defects [22, 23]. The strong nitrogen-vacancy binding also facilitates the formation of oxygen clusters. Oxygen clusters and *D*-defects co-exist in a nitrogen-doped crystal (Figure 9). The oxygen-cluster-free zone near the surface of a wafer after annealing is typically deeper than the *D*-defect-free zone; hence, the presence of oxygen clusters does not add additional annealing time. Moreover, in the bulk of the wafer, far away from the front and the back surfaces of a wafer, oxygen clusters remain in higher densities and provide sites for the precipitation of metallic impurities during microelectronic device fabrication. Thus, nitrogen doping provides dual benefits of the reduction in the size of *D*-defects and of the capability to precipitate metals far away from the wafer surfaces [28].

Since many silicon wafers are not annealed and not produced from nitrogen-doped crystals, they do not contain oxygen clusters in higher densities to facilitate metals precipitation during device fabrication. In such wafers, a desired oxygen cluster density profile can be created, from the front surface to the back surface, by the patented MDZ process [29]. This process starts with a rapid thermal annealing of a wafer (peak temperature around 1225 ^{0}C) to create a high vacancy concentration in the central region of the wafer between its two surfaces. Since oxygen clusters are formed readily in the presence of vacancies, another oxygen cluster growth cycle creates stable oxygen clusters in the bulk of the wafer (Figure 10).

Another popular process that allows the creation of a large-microdefect-free zone near the front surface of a wafer is silicon epitaxy. Silicon epitaxy involves the chemical deposition of silicon from TCS on silicon wafers, according to Reaction (1). Since this chemical vapor deposition (CVD) is strongly influenced by the transport of the reacting species, the manipulation of the reactor geometry and the gas flow dynamics is critical in achieving uniform deposition [30]. The deposited silicon layer is free of large microdefects. Different imperfections can develop within the deposited silicon layer, if large oxygen clusters are present near the surface of the silicon substrate. Hence, a good control of the crystal growth process, especially in the presence of nitrogen, becomes important to achieve the desired quality of the deposited silicon layer.

Defect engineering of silicon wafers is a very vast field that provides limitless opportunities for improvement in the performance of microelectronic devices. Particularly, technologies involving the creation and transfer of different layers provide significant advantages. Silicon on Insulator (SOI) technology is among the most promising emerging technologies. SOI substrate is a layered structure consisting of a top silicon layer free of large microdefects, an intermediate silicon dioxide layer known as the buried oxide layer, and the bottom silicon substrate of average quality. An SOI substrate can be used instead of a conventional silicon substrate for the manufacture of microelectronic devices. The silicon junction built on the SOI substrate is directly above the oxide layer. The isolation from the bulk silicon is reported to reduce parasitic capacitance allowing higher performance for a given power. The SOI substrate also provides resistance to latch up because of the isolation of n- and p-well structures. Figure 11 describes a typical production of an SOI substrate. First, oxide layers of desired thickness are grown on the so-called handle wafer and the so-called donor wafer. The donor wafer is free of large microdefects. Then, ions of a gas such as helium or hydrogen are implanted into the donor silicon wafer [2]. After ion implantation, the oxidized surfaces of the handle and the bulk wafer are bonded at room temperature. Another heat treatment allows the separation of the donor wafer from the SOI substrate. A subsequent heat treatment can strengthen the bond between the two facing oxide layers. The thickness of the donor layer and the oxide layer vary depending on the application. SOI represents one of many emerging materials that can improve the performance of microelectronic devices.

Conclusions

Silicon is the most popular substrate used in the fabrication of microelectronic devices. It played a crucial role in catalyzing the electronic and information technology revolution in the second half of the 20th century. Today, silicon is also the most popular substrate used in the fabrication of solar cells. Hence, silicon is poised to play a key role in the energy technology revolution in the 21st century. Semiconductor silicon processing and solar silicon processing are intricately coupled by common unit operations and physical phenomena at different scales. Today, the business dynamics of the silicon processing industry is unique because it is expected to simultaneously meet the increasing demand from the solar industry and the stringent quality requirements of the semiconductor industry.

As the demand for raw silicon known as polysilicon has significantly increased, the option of producing polysilicon in fluidized bed reactors (FBRs) has become attractive. Silicon from silane is chemically deposited on silicon particles in FBRs. FBRs significantly improve the polysilicon productivity by providing excellent gas-solid contact and volumetric particle surface area. An efficient operation of FBRs requires a deep understanding of multiphase reactive flows. Polysilicon is used to produce silicon single crystals by the Czochralski (CZ) process for semiconductor applications. Various crystallographic imperfections known as microdefects can evolve in a CZ silicon crystal during its growth. Large microdefects adversely affect the fabrication of microelectronic devices. The production of CZ crystals free of large microdefects is among the most significant challenges in CZ crystal growth. To produce a CZ crystal of desired quality, a clear understanding of the reactive transport phenomena in both the melt and the crystal is required. Czochralski single crystals are first sliced into wafers; and the sliced wafers are then treated by various mechanical shaping processes, chemical etching, and surface polishing. Finished substrate wafers must meet more than 2000 specifications that address their materials properties, mechanical properties, and geometric features. A few of these requirements can be met cost-effectively by engineering microdefects in polished wafers. Different options for defect engineering after wafer polishing involve high temperature annealing to reduce the size of microdefects near the wafer surfaces, silicon epitaxy to deposit a microdefect free silicon layer, vacancy assisted controlled oxygen precipitation, and the fabrication of many new materials. The SOI (Silicon on Insulator) substrate appears to offer significant advantages over the traditional silicon substrate for semiconductor applications.

Solar silicon processing starts with the production of polysilicon. Sophisticated single crystal growth is not required for the production solar silicon substrate. Silicon multicrystals are produced by the directional solidification. These multicrystals are cut into rectangular blocks and sliced into wafers. Solar wafers are etched before they are ready for the fabrication of solar cells. Quality specifications for solar wafers are not as numerous as they are for semiconductor wafers. The challenges in silicon processing for solar applications center around improving process efficiencies and productivities.

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Figures

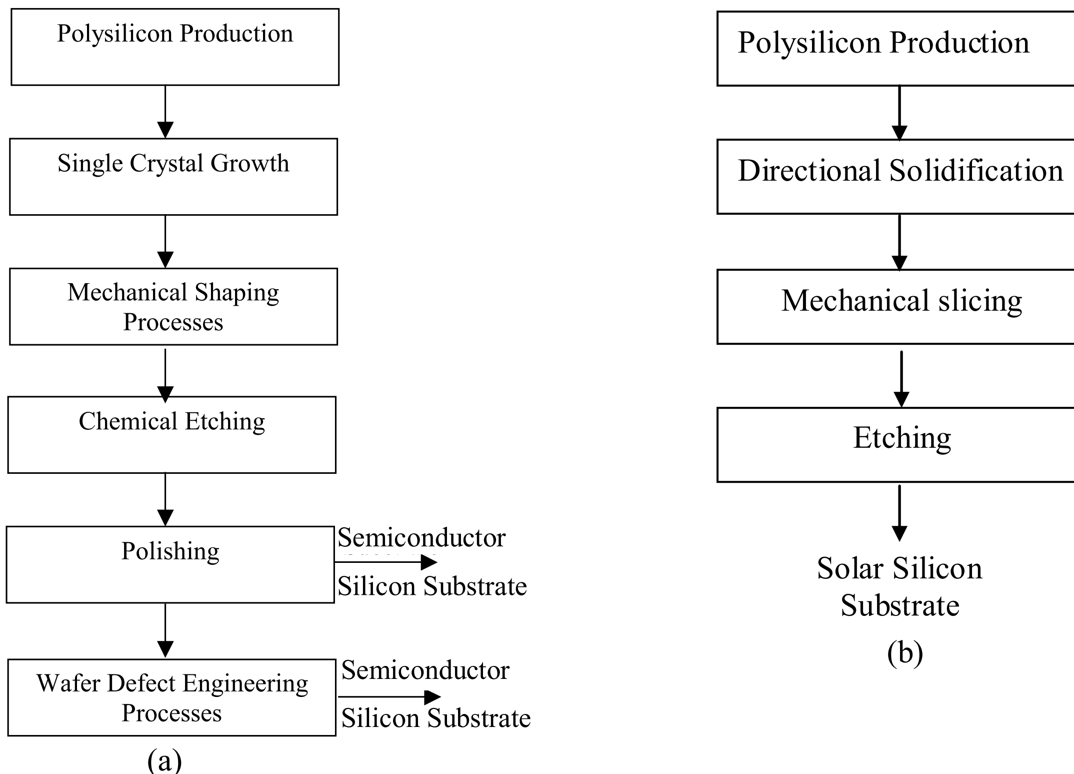


Figure 1. Typical process flow for the production of (a) semiconductor silicon substrate wafers, (b) solar silicon substrate wafers

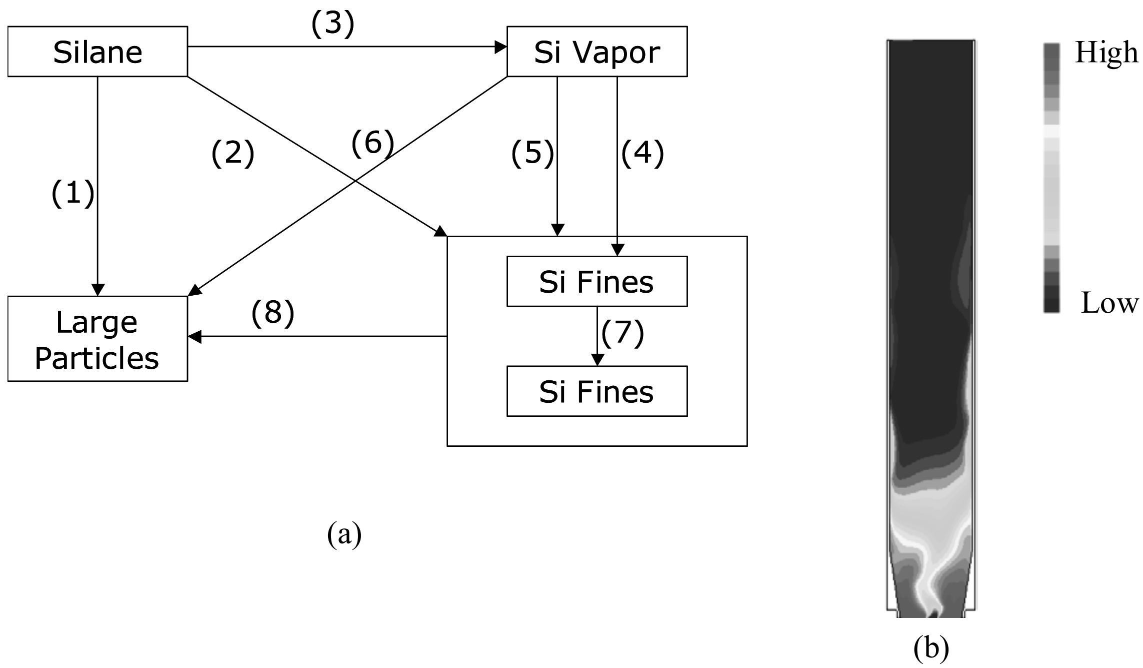


Figure 2. (a) Key reaction pathways in silane-silicon system [3], (b) A snapshot of the predicted mass-fraction field of silane in a typical fluidized bed reactor. Note that the dynamics of fluidized bed reactors is inherently chaotic in nature.

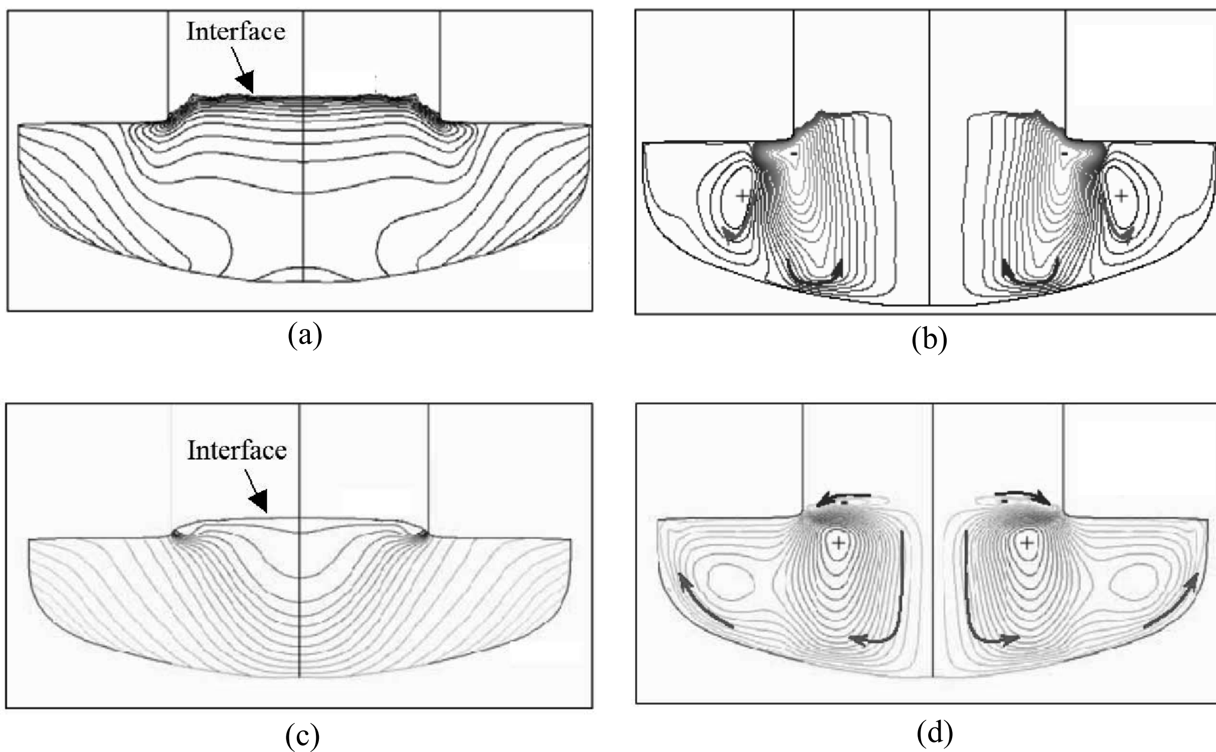


Figure 3. (a) Typical temperature field in silicon melt in the CZ process under the co-rotation condition, (b) Typical flow (stream function) field in silicon melt in the CZ process under the co-rotation condition, (c) Typical temperature field in silicon melt in the CZ process under the counter-rotation condition, (d) Typical flow (stream function) field in silicon melt in the CZ process under the counter-rotation condition

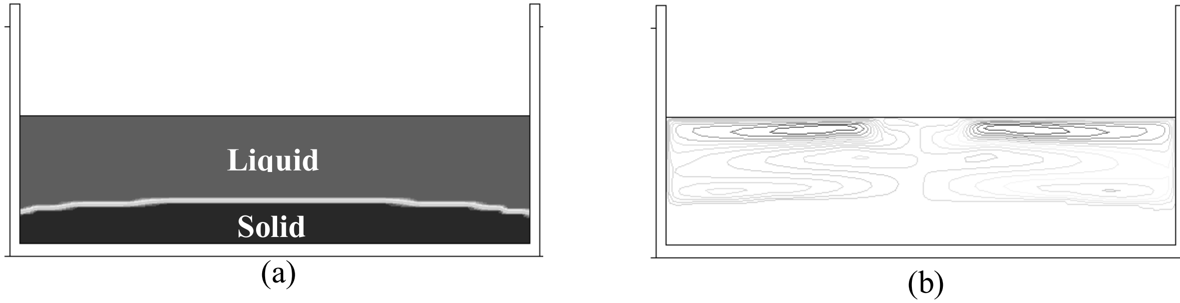


Figure 4. (a) Typical solidification front in the directional solidification process, (b) The predicted stream functions in the melt during a directional solidification. Note that the details of geometry and scale are not shown to protect proprietary information.

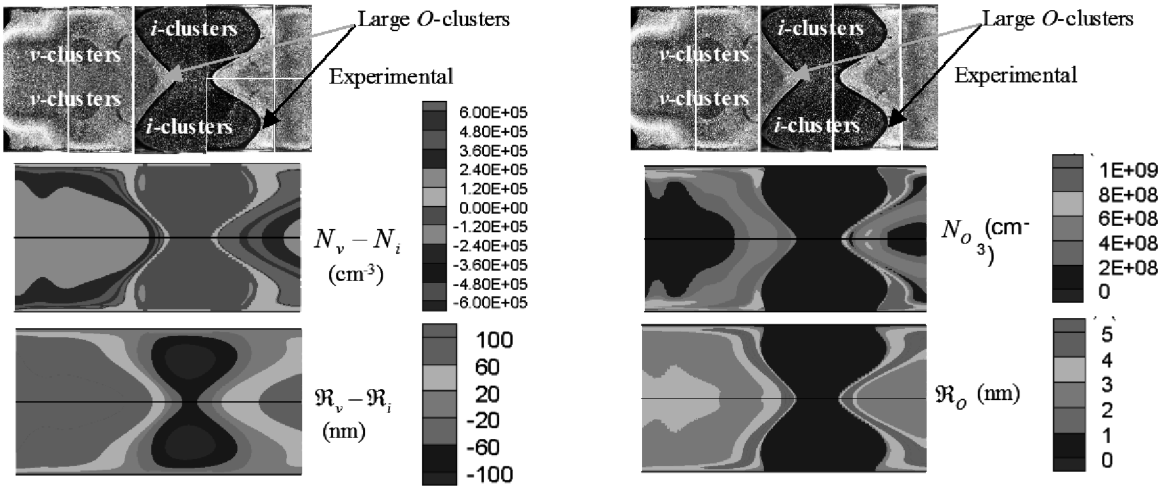
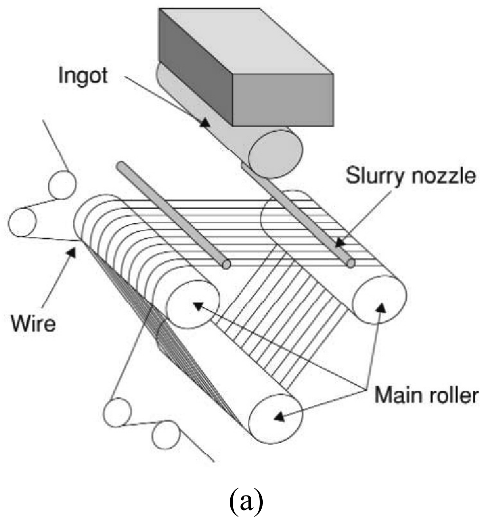
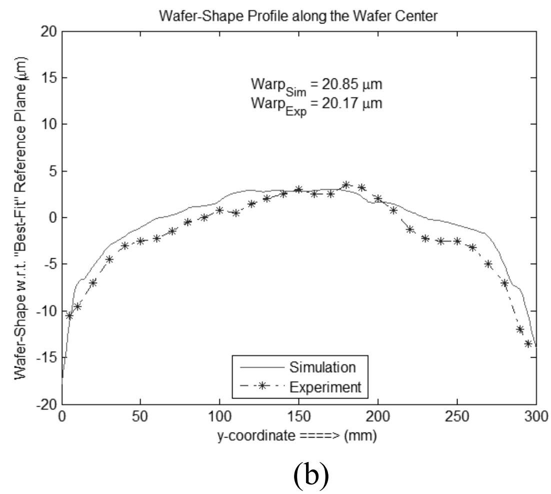


Figure 5. A comparison of the predicted defect distribution in a CZ crystal with the experimental observation. N is the density of microdefects, and $\Re$ is the representative radius of microdefects. The subscript i represents i-clusters, v represents v-clusters, and O represents O-clusters [21].

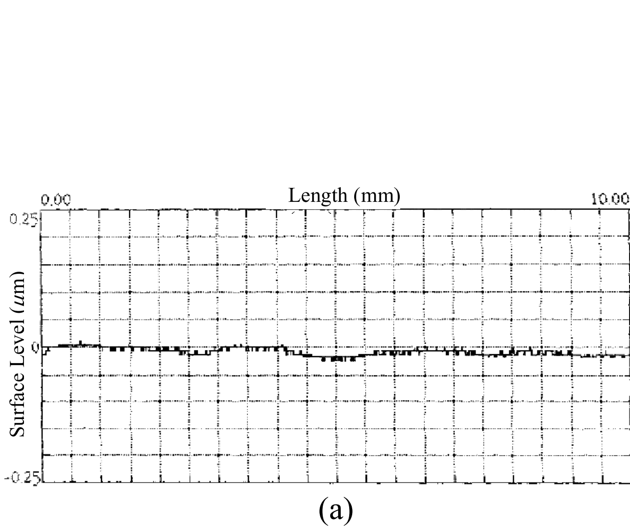


(a)

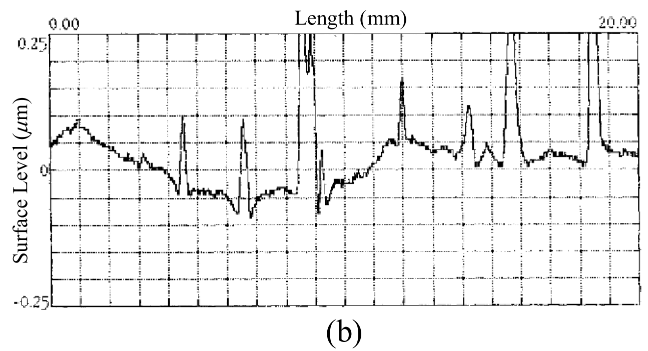


(b)

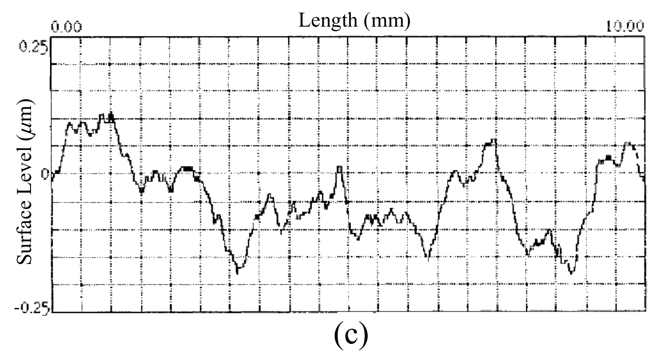
Figure 6. (a) A geometric description of the wire-slicing operation, (b) The predicted warp and the observed warp of a sliced wafer [24].



(a)

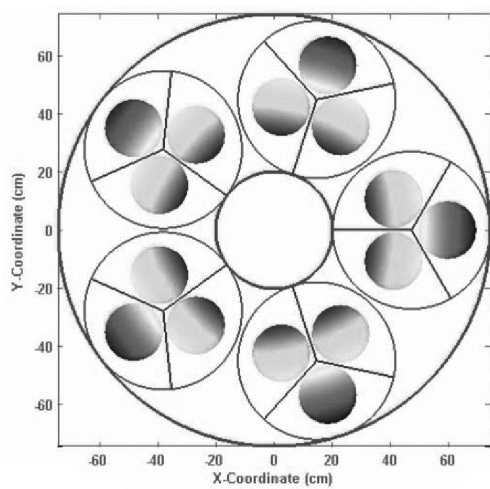


(b)

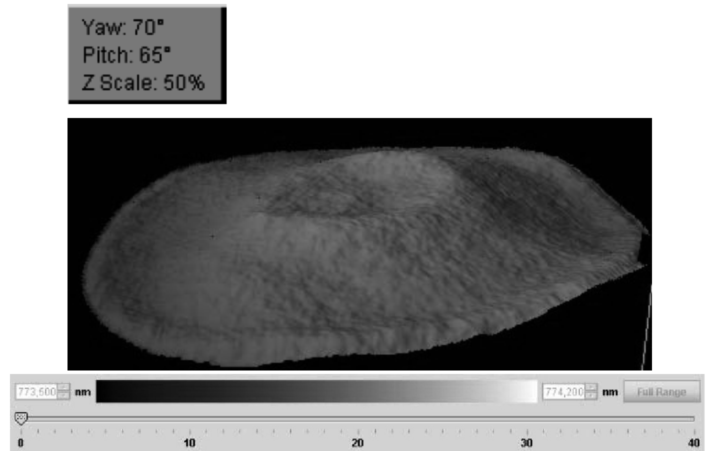


(c)

Figure 7 (a) The qualitative surface profile of a smooth polished wafer, (b) The qualitative surface profile of a wafer etched without extrinsic bubbling, after polishing, (c) The qualitative surface profile of a wafer etched in the presence extrinsic bubbling, after polishing. [27]. Note that polishing follows etching in silicon processing. These experiments were conducted only to show the surface deterioration caused by etching.



(a)



(b)

Figure 8. (a) A schematic of the double side polishing process. Wafers rotate about three axes in this process to achieve surface uniformity, (b) The topography of a polished wafer.

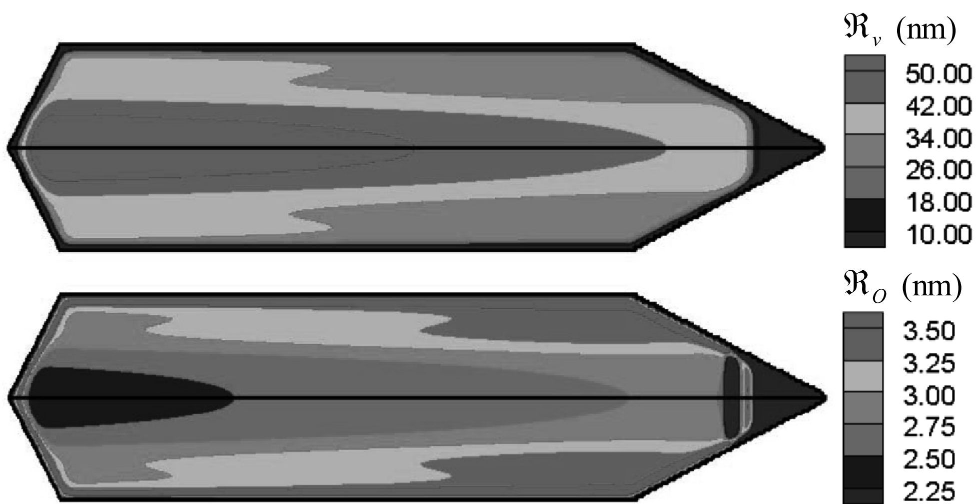


Figure 9. The model predicted cluster distributions in a nitrogen doped CZ crystal, pulled at a fixed rate well above the pull rate at the critical condition, at the end of its growth. Note: The melt/crystal interface is not flat. The total nitrogen concentration varies from 8.25×10^{13} cm^{-3} to 6.7×10^{14} cm^{-3} from one end (LHS) of the crystal to the other (RHS) and from 8.4×10^{13} cm^{-3} to 3.9×10^{14} cm^{-3} along the central axis of the cylindrical body of the crystal; oxygen concentration = 16 ppma. The crystal cooling rates are moderate. The legend for each plot is on its right hand side [23].

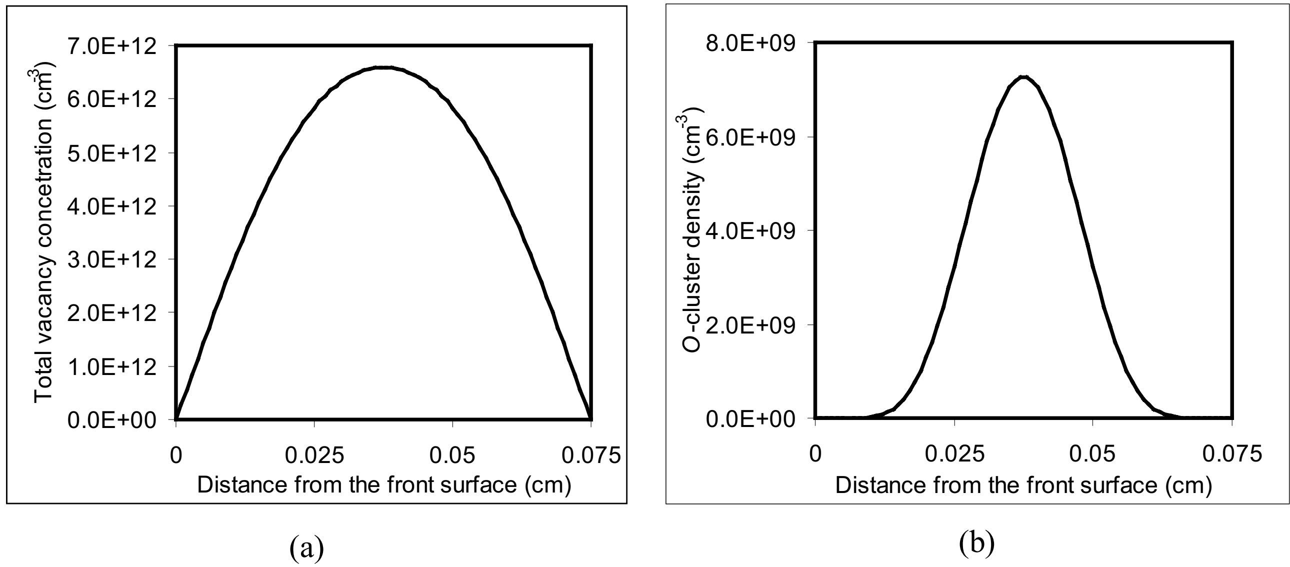


Figure 10. (a) The predicted vacancy concentration profile in a wafer after an MDZ treatment, (b) The oxygen cluster density profile in the wafer after a growth heat cycle

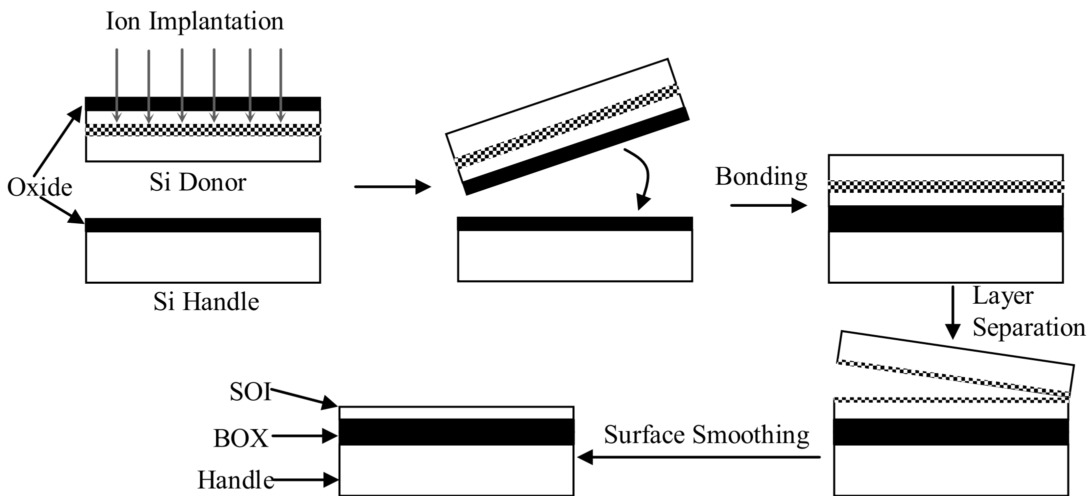


Figure 11. A schematic representation of the production of an SOI substrate